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EXAMINER	
TRINH, MICHAEL MANH	
ART UNIT	**PAPER NUMBER**
2822	
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/799,877	KIM, SI-BUM	
	Examiner	Art Unit	
	Michael Trinh	2822	

-- *The MAILING DATE of this communication appears on the cover sheet with the correspondence address* --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *02 February 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *2,3 and 5-21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *2,3 and 5-21* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

*** This office action is in response to Applicant's Amendment filed February 02, 2007 Claims 2-3,5-21 are pending, in which new claims 19-21 have been added.

*** The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

*** Claim 18 is objected as it should depend on claim 17, since "a second barrier metal" is recited in claim 17, not claim 16.

Claim Rejections - 35 USC § 112

1. Claims 2,3,5-7,19-21 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Re claims 6 and 20, "..the first and the second electrodes..." are lacking antecedent basis.

Re claims 7 and 21, "...the dielectric layer.." is lacking antecedent basis.

Re claims 2,3, the phrase "...wherein the capacitor is formed in the same layer with the first metal interconnection..." is unclear and indefinite since it is the same layer of which layer. (Dependent claims 5-7,19-21 are also rejected as depending on rejected base claim)

Claim Rejections - 35 USC § 102

2. Claim 2 is rejected under 35 U.S.C. 102(b) as being anticipated by Hu (6,281,541).

Re claim 2, Hu teach (at Figs 1-12; col 2, line 15 through col 4) a method for forming a semiconductor device comprising: forming an insulation layer 24 in a capacitor region and a metal interconnection region on a substrate 10 (Fig 1; col 2, lines 1-30); forming a first trench 25 at the capacitor region of the insulation layer 24 (Fig 2; col 2, line 30+); forming the first metal interconnection 30 inside the first trench; forming a second trench 35 by removing the insulation layer 24 between the first metal interconnection 30 (Fig 4; col 2, lines 44-53); and forming a capacitor in the second trench (Figs 5-10; col 2, line 50 through col 3); and forming a second metal interconnection 52 over the first metal interconnection 30; wherein the capacitor is formed in the same layer with the first metal interconnection 30 (Figs 4-12).

Claim Rejections - 35 USC § 103

3. Claims 2-3,5-7,16-18,19-21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sung et al (6,346,454) taken with Hu (6,281,541).

Re claim 2, Sung et al. teach a method for forming a semiconductor device comprising at least the steps of: forming an insulation layer 42/40/38 in a capacitor region and a metal interconnection region on a substrate 30 (Figs 1; col 3, line 65 through col 4); forming a first trench at the capacitor region of the insulation layer (Figs 2-5; col 5, line 19 through col 6); forming a first metal interconnection 52/54 inside the first trench (Figs 5-6; col 6, lines 12-57); forming a capacitor in the trench (Figs 7-8; col 6, line 45 through col 7); and forming a second metal interconnection 50 over the first metal interconnection (Figs 6-7; col 6, lines 29-67, 51-58), wherein the capacitor is formed in the same layer with the first metal interconnection 52/54 (Fig 6-8). Re claim 3, Sung et al. teach a method for forming a semiconductor device comprising at least the steps of: forming an insulation layer 42/40/38 in a capacitor region and a metal interconnection region on a substrate 30 (Figs 1; col 3, line 65 through col 4); forming a first trench at the capacitor region of the insulation layer (Figs 2-5; col 5, line 19 through col 6); forming a first barrier metal 52 and the first metal interconnection 54 inside the first trench (Figs 5-6; col 6, lines 12-57); forming a second trench by removing the insulation layer around the first barrier metal 52; forming a third trench in the first barrier metal 52 by removing the first metal interconnection 54 in the first barrier metal 52 (Fig 5, col 6, lines 12-28); and forming a capacitor in the third trench (Figs 6-8, col 6, lines 29-67); and forming a second metal interconnection 50 over the first metal interconnection (Figs 6-7; col 6, lines 29-67, 51-58), wherein the capacitor is formed in the same layer with the first metal interconnection (Fig 1-8). Re claim 16, Sung et al. teach a method for forming a semiconductor device comprising at least the steps of: forming an insulation layer 42/40/38 in an metal interconnection region and a capacitor region on a substrate 30 (Figs 1; col 3, line 65 through col 4); forming an interconnection trench in the first metal interconnection and a first trench at the capacitor region by selectively etching the insulation layer (Figs 2-5; col 5, line 19 through col 6); forming a copper interconnection 54, and a first copper interconnection 54 by forming a forming a first barrier metal 52 and a first copper layer 54 in the interconnection trench and the first trench (Figs 5-6; col 6, lines 12-57); forming a third trench in the first barrier metal 52 by selectively etching the first metal interconnection 54

in); and forming a capacitor in the third trench (Figs 6-8; col 6, lines 29-67); and forming a second metal interconnection 50 over the first metal interconnection (Figs 6-7; col 6, lines 29-67, 51-58), wherein the capacitor is formed in the same layer with the first metal interconnection (Fig 1-8). Re claims 5,19, wherein the first metal interconnection 54 comprises a copper (col 4, lines 45-50). Re claims 6,20, wherein material of the electrodes includes tungsten (W) (col 4, lines 45-50). Re claims 7,21, wherein the dielectric layer 46 comprises tantalum oxide (col 4, lines 61-65). Re claim 17, wherein a second barrier metal 42 is formed prior forming the second aluminum copper layer 52 (Figs 12,8-12; col 3, lines 1-30). Re claim 18, wherein the first and second barrier metals 28/42 include titanium nitride (col 2, lines 37-40; col 3, lines 1-5).

Re claims 2-3,16, Sung thus lacks forming a second trench by removing the insulation layer between the first metal interconnection (as in claim 2), around the first barrier metal 52 (as in claim 3), or around the first copper interconnection (as in claim 16). Re claim 16, Sung lacks forming via hole in the insulation layer.

However, re claims 2,3,16, Hu further teaches (at Figs 4,3,5; col 2, lines 45-53; col 2, line 31-67; col 3, lines 37-43)) further forming a second trench 35 by removing the insulation layer 24 around the first metal interconnection 30 and around the first barrier metal 28. Re further claim 16, Hu also teaches (at Figs 2,4,12; col 2, line 31 to col 3) forming a via hole (Fig 2, the most right opening 25) in the insulation layer 24 in addition to forming the interconnection trench 25 and the first trench 25 (other openings 25 in Fig 2).

Therefore, re claims 2,3,16, it would have been obvious to one of ordinary skill in the art at the time the invention was made to form the capacitor of Sung by further forming a second trench by removing the insulation layer around the first metal interconnection and around the first barrier metal, as taught by Hu. This is at least because of the desirability to form a capacitor having a larger capacitor area (Hu at col 3, lines 37-43). Re further claim 16, it would have been obvious to one of ordinary skill in the art at the time the invention was made to form the device of Sung by further forming a via hole in the insulation layer as taught by Hu. This is because of the desirability to provide an another electrical connection to the underlying conductive layer.

4. Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over Hu (6,281,541) taken with Sung et al (6,346,454).

Hu teaches a method for forming a semiconductor device as applied to claim 2 above. Re claim 5, Hu teaches the first metal interconnection 30 comprising a tungsten (col 2, lines 37-40).

Re claim 5, Hu lacks mentioning the first metal interconnection comprising a copper.

However, Sung teaches (col 4, lines 40-50) forming a first metal interconnection 54 by using either a copper, aluminum or tungsten.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to first metal interconnection of Hu by using either a copper, aluminum or tungsten, as taught by Sung. This is because of these conductive materials are alternative and art recognized equivalent conductive materials for forming the metal interconnection, wherein copper is a conductive material having high electrical conductivity.

5. Claim 6-7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hu (6,281,541) taken with Vaartstra et al (6,445,023).

Hu teaches a method for forming a semiconductor device as applied to claim 2 above. Re claim 7, Hu already teaches forming the capacitor dielectric layer 36 of an oxide (col 3, lines 37-50 for metal-oxide-metal; col 2, lines 54-67). Re claim 6, Hu also teaches forming first and second electrodes 30 and 42 (Fig 12; col 3, line 38 through col 4, line 10), wherein tungsten (W) is mentioned at col 2, lines 37-41).

Re claim 6, Vaartstra does not mention first and second electrodes including Pt, Ru, Ir, or W. Re claim 7, Hu thus lacks mentioning other materials of metal oxide dielectric.

However, re claim 6, Vaartstra teach (at col 7, lines 40-50; col 8, lines 1-19; col 6, lines 27-57) forming the first and second electrodes 152,156 of a conductive material including Pt, Ru, Ir. Re claim 7, Vaartstra also teaches (col 7, lines 57-67) employing a dielectric material including tantalum oxide, strontium titanate, and barium titanate, etc.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to the electrodes of Hu by employing the conductive materials including Pt, Ru, and Ir as taught by Hu, because of these conductive materials are alternative and art recognized equivalent conductive materials for forming the electrodes, wherein Pt, Ru, and Ir are

materials having high electrical conductivity. Also, it would have been obvious to one of ordinary skill in the art at the time the invention was made to the dielectric of Hu by using tantalum oxide, strontium titanate, barium titanate, as taught by Vaartstra. This is because of the desirability to form a dielectric having high-k dielectric constant in forming the capacitor.

6. Claims 8,9,15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hu (6,281,541) taken with Sung et al (6,346,454).

Re claim 8, Hu teaches (at Figs 1-12; col 2, line 15 through col 4) a method for fabricating a semiconductor device comprising: forming an insulation layer 24 including a first insulation layer 14 and a second insulation layer 24 in a capacitor region and a metal interconnection region on a substrate formed with a lower conductive layer 22 (Fig 1; col 2, lines 1-36); forming an interconnection trench (most right trench 25 in Fig 2) in the metal interconnection region, a first trench (middle trench 25) in the capacitor region and a via hole (most left trench 25 in Fig 2) connected to the lower conductive layer 22 by selectively etching the insulation layer (Fig 2, col 2, lines 30+); forming a metal interconnection 30 of tungsten, a first metal interconnection 30 and a via contact plug 31 by forming a first tungsten layer in the interconnection trench, the via hole and the first trench (Fig 2-4; col 2, lines 30-52); forming a second trench 35 by selectively etching the second insulation layer 24 in the capacitor region (Fig 4; col 2, lines 44-53); forming a capacitor in the second trench; and forming a barrier layer 42 on the capacitor and a second metal interconnection comprising AlCu (col 3, lines 22-31). Re claim 15, Hu teaches forming a barrier metal layer 28 before forming the first metal layer 30,31 (Figs 3-4; col 2, lines 30-40).

Re claim 5, Hu already teaches forming a first metal interconnection, but lacks mentioning the metal interconnection comprising a copper.

However, Sung teaches (col 4, lines 40-50) forming a first metal interconnection 54 by using either copper, aluminum, or tungsten.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to form the first metal interconnection of Hu by using either copper, aluminum or tungsten, as taught by Sung. This is because of these conductive materials are

alternative and art recognized equivalent conductive materials for forming the metal interconnection, wherein copper is a conductive material having high electrical conductivity.

Re further claim 9, Hu lacks the insulation layer having an etching blocking layer.

However, Sung teaches (at Figs 2-4; col 4, lines 28-51; col 5, line 42 through col 6) etching to form the trench and the via hole in the insulation layer having an etching blocking layer 40 between the first insulation layer 38 and the second insulation layer 42.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to form the insulation layer of Hu by forming the insulation layer having an etching blocking layer between the first insulation layer and the second insulation layer. This is because of the desirability to use the etching blocking layer as an etch stop layer to protect the underlying layer during the etching step to form the trench and via hole.

7. Claims 10,13-14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hu (6,281,541) taken with Sung et al (6,346,454), as applied to claims 8,9,15, and further of Raajimakers (6,686,271).

The references including Hu and Sung teach (at Figs 1-12; col 2, line 15 through col 4) a method for fabricating a semiconductor device as applied to claims 8,9,15 above.

Re claim 10, the references including Hu and Sung lack employing the insulation layer having a hard mask on a second insulation layer. Re claims 13-14, the references including Hu and Sung lack forming the copper layers by using reflow method and, in case of using electroplating, forming a seed layer.

However, re claim 10, Raajimakers teaches forming the trench in the insulation layer having a hard mask layer 58 as etch stop layer on the second insulation layer 56, and having an etching blocking layer 54 between the first insulation layer 50 and the second insulation layer 56 (Figs 8-9,13; col 7, line 55 through col 9), wherein the hard mask layer is also used as a stopper during planarizing step (Fig 13, col 27, lines 7-12). Re claims 13-14, Raajimakers also teaches (at Figs 11-12; col 26, line 48 through col 27, line 5) forming the copper conductive layer 160 use a reflow method after forming a layer such as forming a seed layer by PVD, CVD or electroplating.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to form in the insulation layer of the references including Sung and Hu by employing the insulation layer having a hard mask layer on the second insulation layer, and having an etching blocking layer between the first insulation layer and the second insulation layer, as taught by Raajimakers. This is because of the desirability to use the hard mask layer as a masking layer to protect the underlying layer, and to act a stopper during planarizing step.

The subject matter as a whole would have been obvious to one of ordinary skill in the art at the time the invention was made to form the copper interconnection of the references including Sung and Hu by forming a seed layer prior forming a copper layer by electroplating, as taught by Raajimakers, wherein a seed layer is formed by PVD, CVD or electroplating. This is This is because of the desirability to use the seed layer to facilitate electroplating of the copper interconnection layer in the trench.

8. Claims 11-12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hu (6,281,541) taken with Sung et al (6,346,454), as applied to claims 8,9,15, and further of Huang (6,117,725)

The references including Hu and Sung teach (at Figs 1-12; col 2, line 15 through col 4) a method for fabricating a semiconductor device as applied to claims 8,9,15 above.

Re claims 11-12, the references including Hu and Sung lack mentioning alternative order of forming of the via hole and the trenches.

However, Hu also teaches simultaneously forming the interconnection trench, the first trench, and the via hole. Huang teaches (at Figs 2-3) simultaneously forming the interconnection trench 4 and the first trench 4 (Fig 2; col 5, line 41-64) prior forming the via hole 6 (Fig 3, co 5, line 65 through col 6).

Therefore, the subject matter as a whole would have been obvious to one of ordinary skill in the art at the time the invention was made to form the trenches and via hole of the references including Hu and Sung by simultaneously forming the interconnection trench and the first trench prior forming the via hole, as taught by Huang, or after forming the via hole. This is because of the desirability to form the trench for interconnection, capacitor trench, and via hole

for electrical connection in the insulation layer, wherein the order of carrying out these various steps can be alternatively performed without departing from the spirit of the invention.

Response to Amendment

9. Applicant's amendments and remarks submitted February 02, 2007 with respect to pending claim have been considered but are moot in view of the new ground(s) of rejection.

In the amendment filed February 02, 2007, Applicant amended all base claims including objected claims and even allowed claims in order to broaden scope of all claims. Accordingly, the indication of allowable subject matter in the last office actions is no longer applicable and thereby withdrawn due to Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action.

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Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL.** See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

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Any inquiry concerning this communication or earlier communications from the examiner should be directed to Michael M. Trinh whose telephone number is (571) 272-1847. The examiner can normally be reached on M-F: 9:00 Am to 5:30 Pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Zandra Smith can be reached on (571) 272-2429. The central fax phone number is (703) 872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Oacs-18

Michael Trinh
Primary Examiner